Product Design Guide for

Osbourne IO board

Based on Nvidia AGX Orin Module

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Revision	Date	Comment
0.1	22 Feb 2023	Initial Release

Table of Contents

1. INTRODUCTION

This document is intended as a guide for designing a Custom I/O board for Osbourne base board. Osbourne is a Jetson AGX Orin module-based board with rich graphics and camera input capability. Osbourne board converts Jetson AGX Orin module into a complete embedded system by providing interface circuitry, I/O connector for all the major features of the module, camera interface, power supply and additional I/O capability.

I/O connector provides flexibility to users to design custom boards based on the application like commercial IO boards or Rugged latching connector-based IO boards.

This document details the features available on IO connector only. Refer Osbourne user manual to get more details on features mapped on to the other connectors on the Osbourne base board.

1.1 I/O Features and Connector Type

All the I/O signals are routed to a 150pin single I/O Connector board with all circuitries included in the Osbourne base board to have only Passive connectors and minimal components on custom I/O board developed by third parties.

Main I/O Features	Description
Power	7V-20V wide input supply, typical18 V
RTC	3V power input for RTC functionality
USB	4x USB 2.0, 3x USB 3.2
Ethernet	1G/2.5G/5G/10G Multi Mode Gigabit Ethernet without on board Magnetics
	10/100/1000Mbps through RGMII adapter board without on board Magnetics
Audio	Via ALC5640 CODEC
Serial ports	2 x ports Software configurable RS-232/422/485 through SP336 transceivers with bypass option to access TTL signals
	2x ports fixed RS-232 through SP3243 transceivers with bypass option to access TTL signals
Display	1x HDMI 2.0a/b or DP directly from the Module
Digital IOs	8 Digital IO via I2C to GPIO
CAN	2x CAN with Non isolated transceivers
Utility	PWR_ON, RESET, FORCE RECOVERY, MEM_ERASE, I2C, SPI

1.2 Reference

- Osbourne User Manual
  https://www.diamondsystems.com/files/binaries/Osbourne%20user%20manual%20v0.3%2020230105.pdf
- Nvidia AGX Orin product design guide
  https://developer.nvidia.com/embedded/secure/jetson/agx_orin/jetson_agx_orin_design_guide_dg-10653-001_v0.2.pdf

1.3 Block Diagram

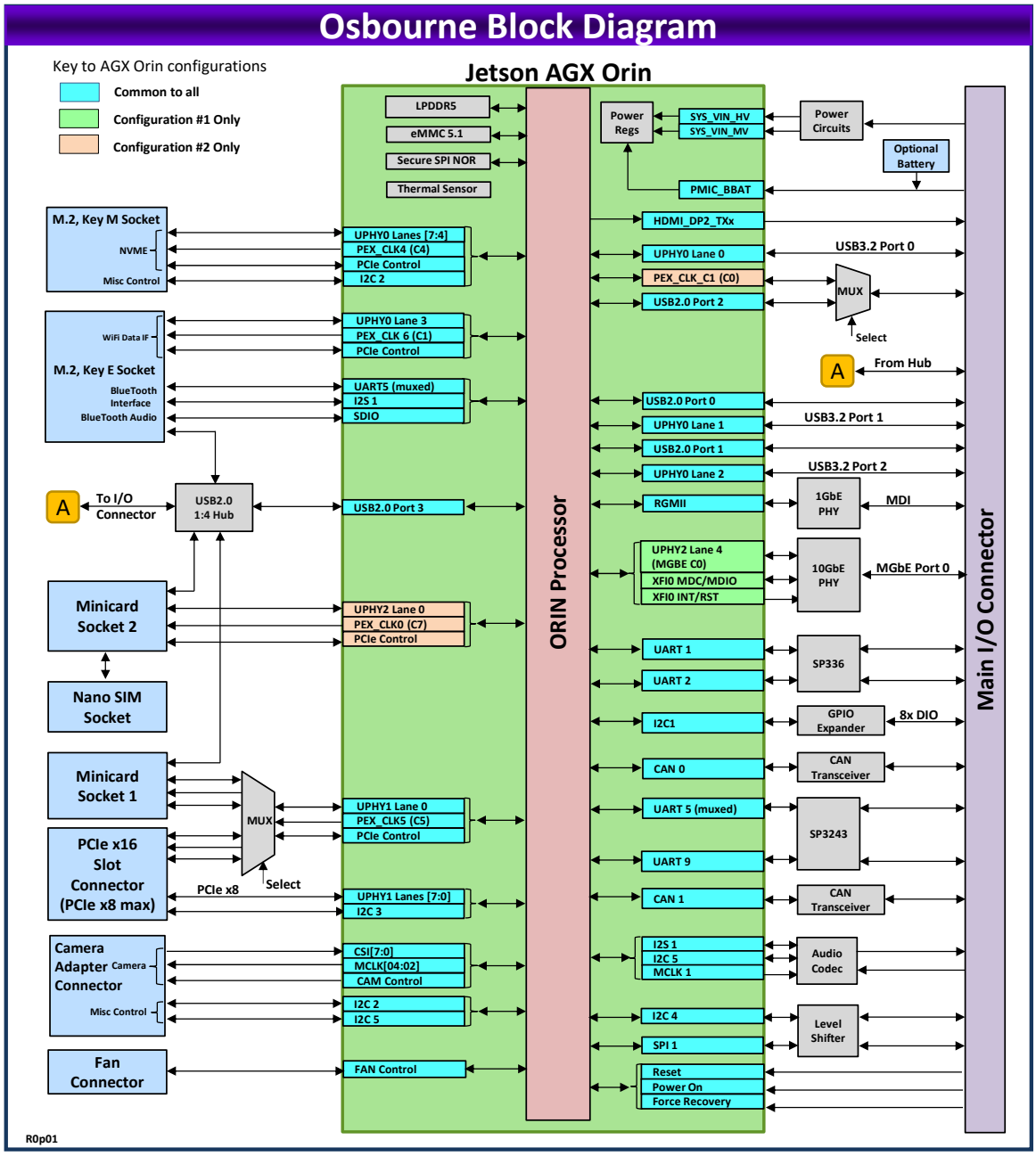

Figure 1: Osbourne Block Diagram

1.4 IO Connector Pinouts

Odd Row Pinouts

Pin#	Signal Name	Voltage Level/Pin Type	Direction wrt Baseboard	Orin Module Pin#
1	AUDIO_HPOR_HDA	Analog Output	Output	NA
3	AUDIO_HPOL_HDA	Analog Output	Output	NA
5	V_3P0_RTC_CON	Power: 1.8V to 3.46V	Input	NA
7	V_5P0_A	Power: 5.0V	Output	NA
9	V_DIO	Power: 3.3V /5.0 V	Output	NA
11	DIO_PA7	V_DIO	Bi-directional	NA
13	DIO_PA6	V_DIO	Bi-directional	NA
15	DIO_PA5	V_DIO	Bi-directional	NA
17	DIO_PA4	V_DIO	Bi-directional	NA
19	DIO_PA3	V_DIO	Bi-directional	NA
21	DIO_PA2	V_DIO	Bi-directional	NA
23	DIO_PA1	V_DIO	Bi-directional	NA
25	DIO_PA0	V_DIO	Bi-directional	NA
27	V_USB3_1	Power: 5.0V	Power	NA
29	USB2_D1_CH_N	USB2 Diff pair	Bi-directional	C10
31	USB2_D1_CH_P	USB2 Diff pair	Bi-directional	C11
33s	V_USB3_2	Power: 5.0V	Output	NA
35	USB2_D0_CH_N	USB2 Diff pair	Bi-directional	F13
37	USB2_D0_CH_P	USB2 Diff pair	Bi-directional	F12
39	GPIO20_DP/HDMI_EN_1P8	1.8 V	Output	A58
41	DP2_AUX_CH_P	Open-Drain, 1.8V (3.3V tolerant)	Output	G53
43	DP2_AUX_CH_N	Open Drain, 1.8V (3.3V tolerant	Bi-directional	G54
45	HDMI_CEC_CON	Open Drain, 1.8V (3.3V tolerant	Bi-directional	J50
47	DP2/HDMI_HPD	CMOS – 1.8V	Input	K50
49	UART5_CTS_RS232	RS232 Signal	Input	NA
51	UART5_RX_RS232	RS232 Signal	Input	NA
53	UART5_RTS_RS232	RS232 Signal	Output	NA
55	UART5_TX_RS232	RS232 Signal	Output	NA
57	UART3_9_RX_RS232	RS232 Signal	Input	NA
59	UART3_9_TX_RS232	RS232 Signal	Output	NA
61	V_USB2_VBUS	Power: 5.0V	Power	NA
63	USB2_HUB_D4_CH_N	USB2 Diff pair	Bi-directional	NA
65	USB2_HUB_D4_CH_P	USB2 Diff pair	Bi-directional	NA
67	V_USB3_3	Power: 5.0V	Power	NA
69	USB2/PCIE_CLK_CH_N	USB2 Diff pair/ PCIe Diff pair	Bi-directional	A11/F17
71	USB2/PCIE_CLK_CH_P	USB2 Diff pair/ PCIe Diff pair	Bi-directional	A10/F16
73	CAN1_L	CAN Differential Pair	Bi-directional	NA
75	CAN1_H	CAN Differential Pair	Bi-directional	NA
77	CAN0_L	CAN Differential Pair	Bi-directional	NA
79	CAN0_H	CAN Differential Pair	Bi-directional	NA
81	CTS2/RX2_N	RS232/ RS422	Input	NA
83	RX2/RX2_P	RS232/ RS422	Input	NA
85	RTS2/TX2_N/RX2_N	RS232/ RS422/ RS485	Bi-directional	NA
87	TX2/TX2_P/RX2_P	RS232/ RS422/ RS485	Bi-directional	NA
89	CTS1/RX1_N	RS232/ RS422	Input	NA
91	RX1/RX1_P	RS232/ RS422	Input	NA
93	RTS1/TX1_N/RX1_N	RS232/ RS422/ RS485	Bi-directional	NA
95	TX1/TX1_P/RX1_P	RS232/ RS422/ RS485	Bi-directional	NA
97	I2C_GP8_DAT_3P3	I2C data; 3.3 V	Bi-directional	E60
99	I2C_GP8_CLK_3P3	I2C Clock; 3.3 V	Output	D61
101	BUTTON_POWER_ON_N	3.3 V	Input	L61
103	SYS_RST_IN_N	Open Drain, 1.8V	Bi-directional	L60
105	FORCE_RECOVERY#	CMOS – 1.8V	Input	L10
107	No Connection			
109	No Connection			
111	PEX_C1_RST_N	Open-Drain, 3.3V	Output	B9
113	MEM_ERS_GPIO	1.8 V	Input	NA
115	SER_GPIO_SEL	1.8 V	Output	A48
117	CAN_SER_SEL2	1.8 V	Output	H52
119	CAN_SER_SEL1	1.8 V	Output	D54
121	SPI1_SCK_3P3	3.3 V	Output	J57

123	SPI1_CS0_3P3	3.3 V	Output	E55
125	SPI1_MISO_3P3	3.3 V	Input	A56
127	SPI1_MOSI_3P3	3.3 V	Output	D55
129	KSZ_LED2	1.8 V	Output	NA
131	KSZ_LED1	1.8 V	Output	NA
133	MGBE_LED2	Open Drain, 20mA	Output	NA
135	MGBE_LED1	Open Drain, 20mA	Output	NA
137	MGBE_LED0	Open Drain, 20mA	Output	NA
139	V_3P3	Power: 3.3V	Output	NA
141	GND_DIG	Ground	Ground	NA
143	V_VIN	Power: 7-20V	Input	NA
145	V_VIN	Power: 7-20V	Input	NA
147	V_VIN	Power: 7-20V	Input	NA
149	V_VIN	Power: 7-20V	Input	NA

Even Row Pinouts

Pin#	Signal Name	Voltage Level/Pin Type	Direction wrt Baseboard	Orin Module Pin#
2	GND_AUD	Audio Ground	Ground	NA
4	AUDIO_MIC_L	Analog Input	Input	NA
6	AUDIO_MIC_R	Analog Input	Input	NA
8	AUDIO_PRSNT_L	1.8 V	Input	NA
10	GND_DIG	Ground	Ground	NA
12	USB3/PCIE_UPHY_RX0_P	USB3 / PCIe Diff pair	Input	A22
14	USB3/PCIE_UPHY_RX0_N	USB3 / PCIe Diff pair	Input	A23
16	GND_DIG	Ground	Ground	NA
18	USB3/PCIE_UPHY_TX0_P	USB3 / PCIe Diff pair	Output	J22
20	USB3/PCIE_UPHY_TX0_N	USB3 / PCIe Diff pair	Output	J23
22	GND_DIG	Ground	Ground	NA
24	USB3_UPHY_RX1_P	USB3 Diff pair	Input	C23
26	USB3_UPHY_RX1_N	USB3 Diff pair	Input	C22
28	GND_DIG	Ground	Ground	NA
30	USB3_UPHY_TX1_P	USB3 Diff pair	Output	G23
32	USB3_UPHY_TX1_N	USB3 Diff pair	Output	G22
34	GND_DIG	Ground	Ground	NA
36	HDMI_DP2_TX0_CON_P	HDMI Diff pair	Output	D51
38	HDMI_DP2_TX0_CON_N	HDMI Diff pair	Output	D52
40	GND_DIG	Ground	Ground	NA
42	HDMI_DP2_TX3_CON_P	HDMI Diff pair	Output	C51
44	HDMI_DP2_TX3_CON_N	HDMI Diff pair	Output	C50
46	GND_DIG	Ground	Ground	NA
48	HDMI_DP2_TX2_CON_N	HDMI Diff pair	Output	A50
50	HDMI_DP2_TX2_CON_P	HDMI Diff pair	Output	A51
52	GND_DIG	Ground	Ground	NA
54	HDMI_DP2_TX1_CON_N	HDMI Diff pair	Output	B52
56	HDMI_DP2_TX1_CON_P	HDMI Diff pair	Output	B51
58	GND_DIG	Ground	Ground	NA
60	USB3_UPHY_RX20_P	USB3 Diff pair	Input	C34
62	USB3_UPHY_RX20_N	USB3 Diff pair	Input	C35
64	GND_DIG	Ground	Ground	NA
66	USB3_UPHY_TX20_P	USB3 Diff pair	Output	K32
68	USB3_UPHY_TX20_N	USB3 Diff pair	Output	K33ss
ss	GND_DIG	Ground	Ground	NA
72	NC			
74	NC			
76	NC			
78	NC			
80	NC			
82	NC			
84	NC			
86	NC			
88	NC			

90	NC			
92	NC			
94	GND_DIG	Ground	Ground	NA
96	GBE_MDI0_P	1G Copper Diff pair	Bi-directional	NA
98	GBE_MDI0_N	1G Copper Diff pair	Bi-directional	NA
100	GND_DIG	Ground	Ground	NA
102	GBE_MDI1_P	1G Copper Diff pair	Bi-directional	NA
104	GBE_MDI1_N	1G Copper Diff pair	Bi-directional	NA
106	GND_DIG	Ground	Ground	NA
108	GBE_MDI2_P	1G Copper Diff pair	Bi-directional	NA
110	GBE_MDI2_N	1G Copper Diff pair	Bi-directional	NA
112	GND_DIG	Ground	Ground	NA
114	GBE_MDI3_P	1G Copper Diff pair	Bi-directional	NA
116	GBE_MDI3_N	1G Copper Diff pair	Bi-directional	NA
118	GND_DIG	Ground	Ground	NA
120	MGBE0_PHY_A_P	10G Copper Diff pair	Bi-directional	NA
122	MGBE0_PHY_A_N	10G Copper Diff pair	Bi-directional	NA
124	GND_DIG	Ground	Ground	NA
126	MGBE0_PHY_B_P	10G Copper Diff pair	Bi-directional	NA
128	MGBE0_PHY_B_N	10G Copper Diff pair	Bi-directional	NA
130	GND_DIG	Ground	Ground	NA
132	MGBE0_PHY_C_N	10G Copper Diff pair	Bi-directional	NA
134	MGBE0_PHY_C_P	10G Copper Diff pair	Bi-directional	NA
136	GND_DIG	Ground	Ground	NA
138	MGBE0_PHY_D_P	10G Copper Diff pair	Bi-directional	NA
140	MGBE0_PHY_D_N	10G Copper Diff pair	Bi-directional	NA
142	GND_DIG	Ground	Ground	NA
144	V_VIN	Power: 7-20V	Power	NA
146	V_VIN	Power: 7-20V	Power	NA
148	V_VIN	Power: 7-20V	Power	NA
150	V_VIN	Power: 7-20V	Power	NA

2. IO CONNECTOR DETAILS

The IO connector used on the Osbourne baseboard is from the Samtec ERM8 Right angle series.
https://www.samtec.com/products/erm8-ra?EmailTextbox=&FNameTextbox=&LNameTextbox=&auth=1

Connector used on Osbourne baseboard: **ERF8-075-01-L-D-RA-L-TR**

Mating Connector: **ERM8-075-01-L-D-RA-L-TR** for in-line connector board

ERM8-075-02.0-L-DV-TR for right angle connector board (Part can be changed be based on the mating height)

2.1 IO Connector Pin Orientation

IO connector pin numbering indications are provided below on the Osbourne baseboard.

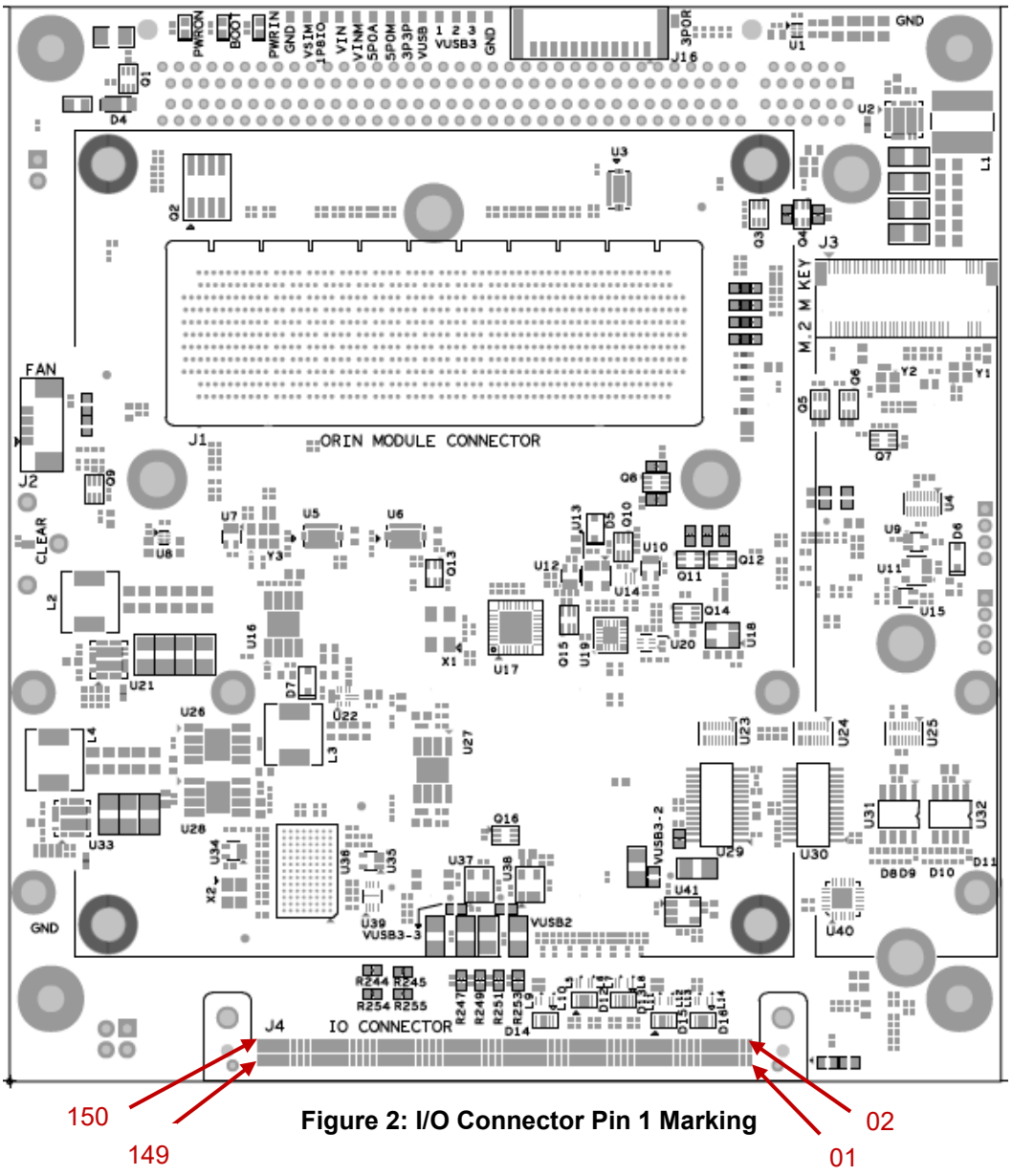

Figure 2: I/O Connector Pin 1 Marking

2.2 IO Connector mated Views

Below screenshot shows the mated view for in-line connector board

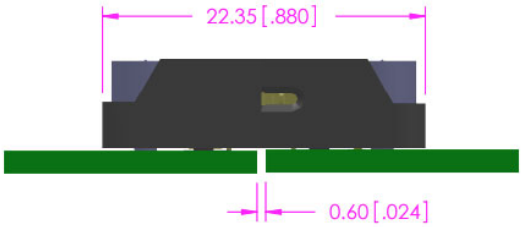

FIG 9
ERF8-RA MATED ERM8-RA

TABLE 16	
Fully Mated Connector to Connector Dimension with Contact Wipe of 1.50[.059]	Max Allowable Connector to Connector Dimension to Maintain Min Contact Wipe of 0.38[.015]
22.35 [.880]	23.47 [.924]

TABLE 17	
Fully Mated Board to Board Dimension with Contact Wipe of 1.50[.059]	Max Allowable Board to Board Dimension to Maintain Min Contact Wipe of 0.38[.015]
0.60 [.024]	1.72 [.068]

Below screenshot shows the mated view for in-line connector board

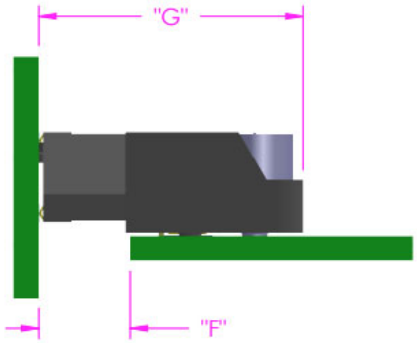

FIG 7
ERF8-DV MATED ERM8-RA

TABLE 12			
		ERM8-RA LEAD STYLE	
		-01	
		"F"	"G"
ERF8-DV LEAD STYLE	-05.0	5.71 [.225]	16.41 [.646]
	-07.0	7.63 [.300]	18.33 [.722]
	-09.0	9.71 [.382]	20.41 [.804]
	-10.0	10.71 [.422]	21.41 [.843]

TABLE 13	
Fully Mated Board to Board Dimension "F" with Contact Wipe of 1.50[.059]	Max Allowable Board to Board Dimension "F" to Maintain Min Contact Wipe of 0.38[.015]
SEE TABLE 12	TABLE 12 DIM "F" + 1.12[.044]

TABLE 14	
Fully Mated Connector to Board Dimension "G" with Contact Wipe of 1.50[.059]	Max Allowable Connector to Board Dimension "G" to Maintain Min Contact Wipe of 0.38[.015]
SEE TABLE 12	TABLE 12 DIM "G" + 1.12[.044]

3. MECHANICAL DRAWINGS

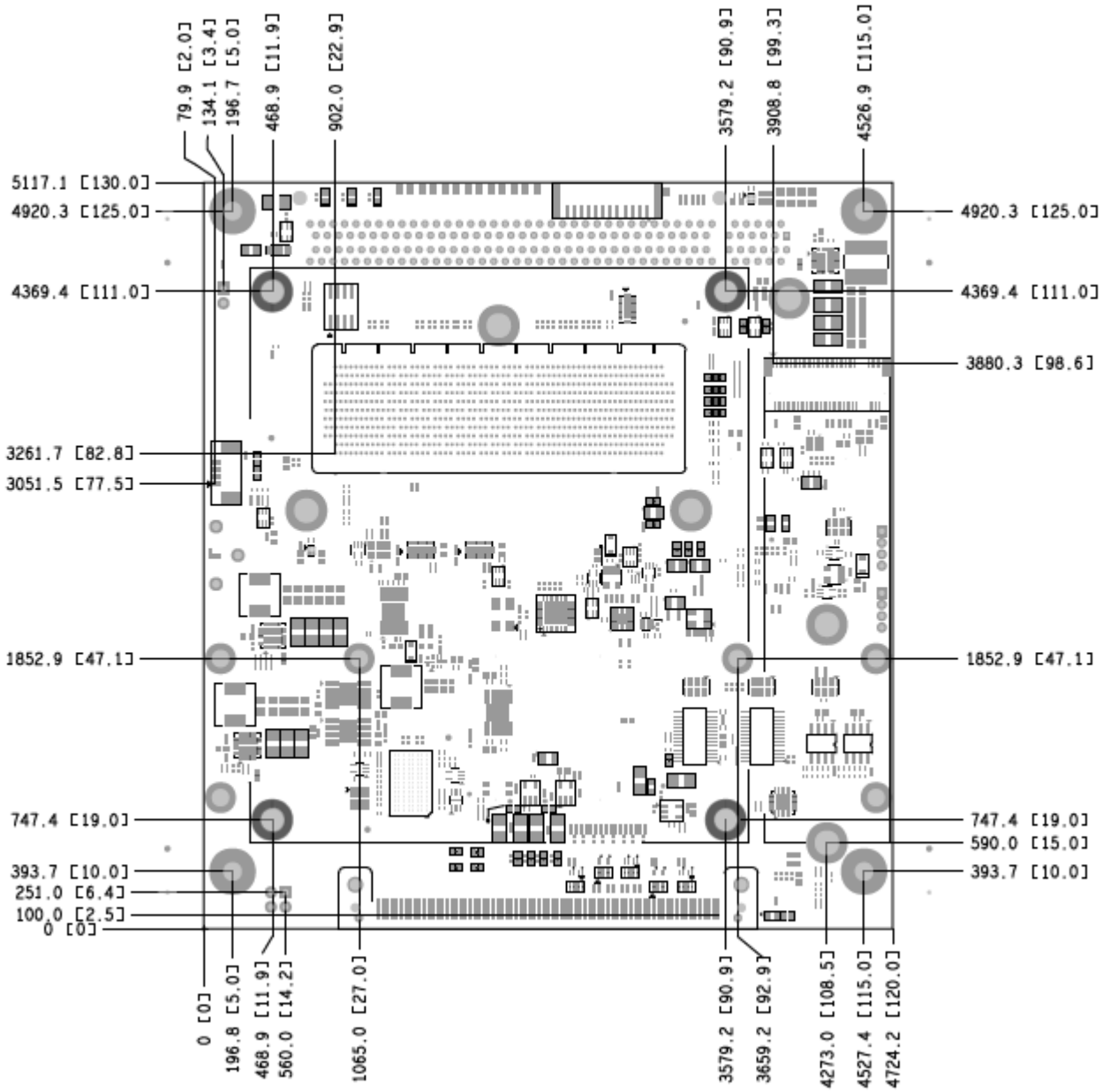

Figure 3: Osbourne Base Board - Top Dimension

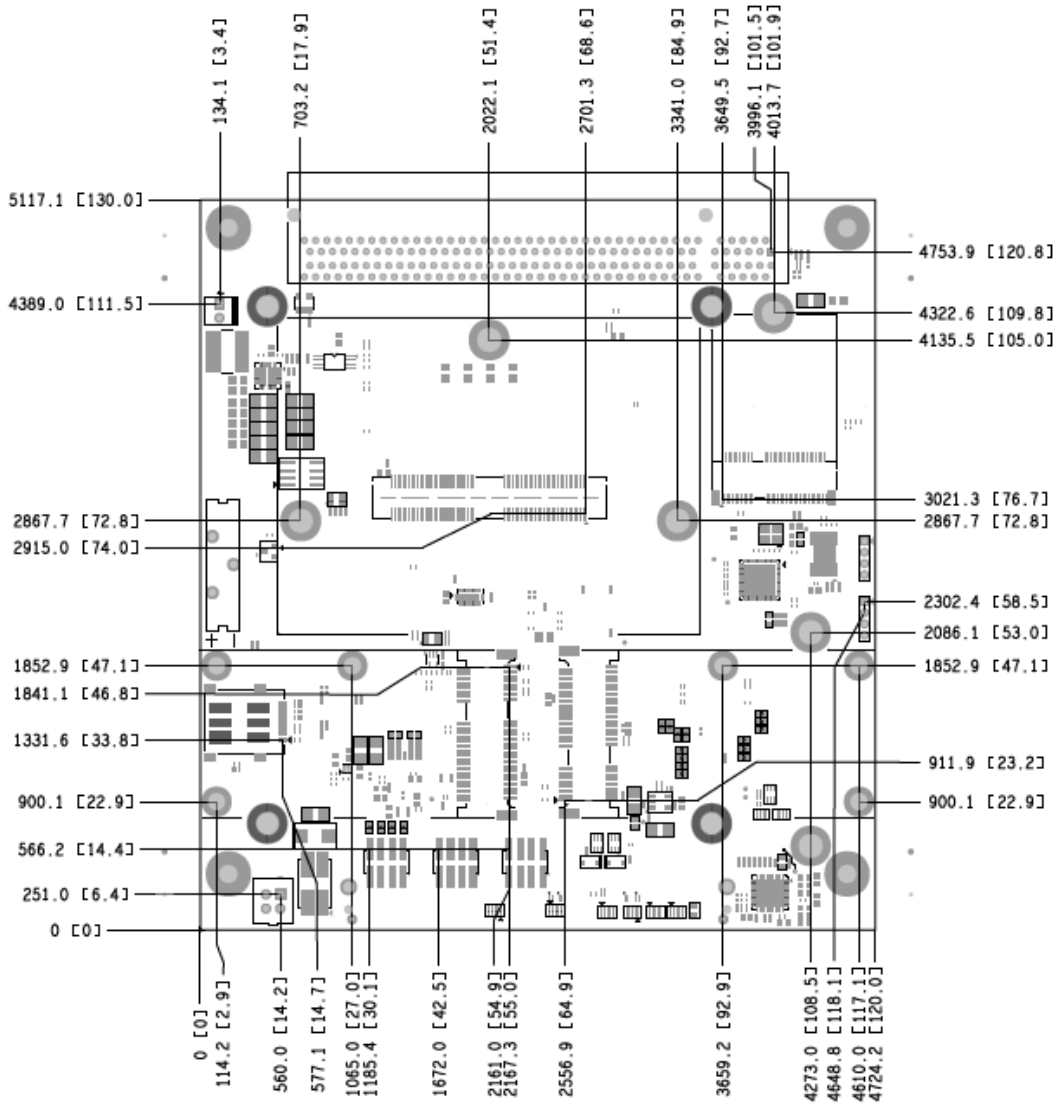

Figure 4: Osbourne Base Board - Bottom Dimension

4. FEATURE DESCRIPTION

4.1.1 Power Supply

The board can be powered from wide input voltage range of +7V to +20V, typically 18V. Supply input should be greater than 15V if PCIe x16 card is being used on the Osbourne board. The supply can be connected to pins 143 through 150 of I/O connector.

Maximum allowable reflected ripple, measured at the voltage input connector is 50mV p-p. Over current protection, Bulk capacitor, EMI filter and reverse protection should be provided on the custom I/O board developed. Refer Figure 5Figure 5: Power Input Sample Circuit for sample input filter circuitry.

The board also provides 5V and 3.3V supplies each with 100mA capacity on the I/O connector.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
143	V_VIN	Power: 7-20V	Connect to 7-20V or typical 18V input, 40W power supply +Ve
145	V_VIN	Power: 7-20V	
147	V_VIN	Power: 7-20V	
149	V_VIN	Power: 7-20V	
144	V_VIN	Power: 7-20V	
146	V_VIN	Power: 7-20V	
148	V_VIN	Power: 7-20V	
150	V_VIN	Power: 7-20V	
7	V_5P0_A	Power: 5.0V	5V, 100mA Output – Can be used for HDMI power
9	V_DIO	Power: 3.3V /5.0 V	3.3V, 100mA Output – Can be used for digital peripheral circuits

Connect supply -Ve to GND pins on the Osbourne board.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
02	GND_AUD	Audio Ground	Connect to Audio ground
10	GND_DIG	Ground	Connect to input power supply -Ve
16	GND_DIG	Ground	
22	GND_DIG	Ground	
28	GND_DIG	Ground	
34	GND_DIG	Ground	
40	GND_DIG	Ground	
46	GND_DIG	Ground	
52	GND_DIG	Ground	
58	GND_DIG	Ground	
64	GND_DIG	Ground	
70	GND_DIG	Ground	
94	GND_DIG	Ground	
100	GND_DIG	Ground	
106	GND_DIG	Ground	
112	GND_DIG	Ground	
118	GND_DIG	Ground	
124	GND_DIG	Ground	
130	GND_DIG	Ground	
136	GND_DIG	Ground	
141	GND_DIG	Ground	
142	GND_DIG	Ground	

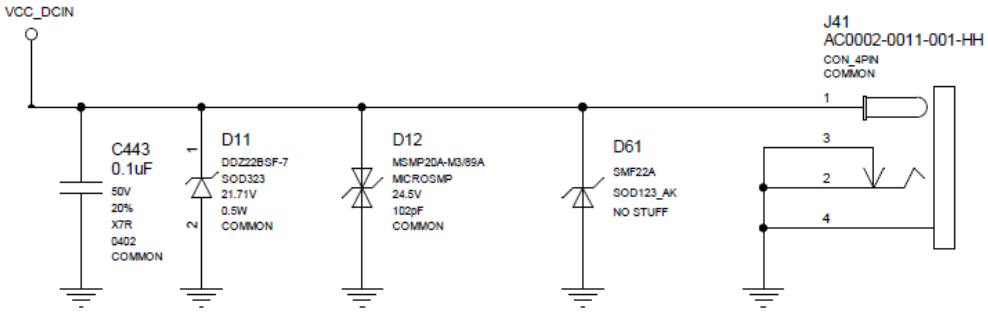

Figure 5: Power Input Sample Circuit

4.2 Backup Battery

RTC of Orin module requires backup voltage from 1.85V to 5.5V max. The backup voltage signal is available on IO connector to connect external backup battery. Connect a Lithium Cell or similar power source. The board supports only non-rechargeable coin cells. The base board can boot and function normally without a backup battery as well. This is achieved by OR'ing circuit implemented on Osbourne base board. Figure 6 shows the OR'ing circuit implementation on Osbourne base board.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
5	V_3P0_RTC_CON	Power: 1.8V to 5.5V	Connect coin cell +Ve to this pin through OR'ing circuit and -Ve to GND

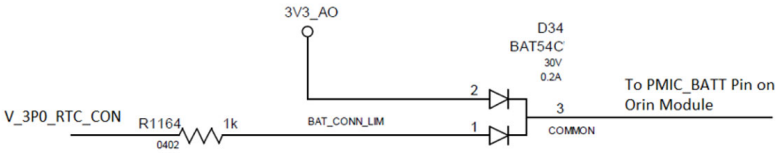

Figure 6: Coin cell OR'ing circuit

Note: 1K series resistor is also available on the Osbourne base board along with OR'ing circuitry.

4.3 Ethernet

The Osbourne board offers Two ethernet port one supports 1G and other supports the 10G ethernet speed.

10G Ethernet port derived using MGBE interface from Orin module using 10G ethernet PHY (part AQR113-B0-I). The Custom I/O board should have 10G magnetics along with the connector. Three LED signals provided for Link, Activity, and Speed Indication.

The 10/100/1000 Ethernet port uses RGMII interface from Orin module through 1G PHY. The Custom I/O board should have 1G magnetics along with the connector. Two LED signals are provided for Link, Activity, and Speed Indication.

Both 10G and 1G port signals are routed to IO connector through following pins.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
96	GBE_MDI0_P	1G Copper Diff pair	Connect to RJ45 pin through a 1G magnetics
98	GBE_MDI0_N	1G Copper Diff pair	
102	GBE_MDI1_P	1G Copper Diff pair	Connect to RJ45 pin through a 1G magnetics
104	GBE_MDI1_N	1G Copper Diff pair	
108	GBE_MDI2_P	1G Copper Diff pair	Connect to RJ45 pin through a 1G magnetics
110	GBE_MDI2_N	1G Copper Diff pair	
114	GBE_MDI3_P	1G Copper Diff pair	Connect to RJ45 pin through a 1G magnetics
116	GBE_MDI3_N	1G Copper Diff pair	
120	MGBE0_PHY_A_P	10G Copper Diff pair	Connect to RJ45 pin through a 10G magnetics

122	MGBE0_PHY_A_N	10G Copper Diff pair	
126	MGBE0_PHY_B_P	10G Copper Diff pair	Connect to RJ45 pin through a 10G magnetics
128	MGBE0_PHY_B_N	10G Copper Diff pair	
132	MGBE0_PHY_C_N	10G Copper Diff pair	Connect to RJ45 pin through a 10G magnetics
134	MGBE0_PHY_C_P	10G Copper Diff pair	
138	MGBE0_PHY_D_P	10G Copper Diff pair	Connect to RJ45 pin through a 10G magnetics
140	MGBE0_PHY_D_N	10G Copper Diff pair	
129	KSZ_LED2	1.8 V Active Low	1G PHY LED2, Refer 4.3.1Figure 7 for more details
131	KSZ_LED1	1.8 V Active Low	1G PHY LED1, Refer 4.3.1Figure 7 for more details
133	MGBE_LED2	Active Low, Open Drain, 20mA	10G PHY LED2, Refer 4.3.2Figure 8 for more details
135	MGBE_LED1	Active Low, Open Drain, 20mA	10G PHY LED1, Refer 4.3.2 for more details
137	MGBE_LED0	Active Low, Open Drain, 20mA	10G PHY LED0, Refer 4.3.2 Figure 8for more details

4.3.1 1G LED Configuration

KSZ_LED2 and KSZ_LED1 configuration is as shown in the following table.

Link/Activity	Pin State		LED Definition	
	LED2	LED1	LED2	LED1
Link Off	H	H	OFF	OFF
1000 Link/No Activity	L	H	ON	OFF
1000 Link/Activity (RX, TX)	Toggle	H	Blinking	OFF
100 Link/No Activity	H	L	OFF	ON
100 Link/Activity (RX, TX)	H	Toggle	OFF	Blinking
10 Link/No Activity	L	L	ON	ON
10 Link/Activity (RX, TX)	Toggle	Toggle	Blinking	Blinking

Note: In Tri-color Dual-LED mode, the KSZ_LED2 and KSZ_LED1 pin outputs toggle high pulses for transmit/receive activity indication. At low data rate (e.g., one frame per second), the LED pin drives high (OFF) with a narrow high pulse width of about 640ns.Typically, the LED toggle rate should be <10Hz (100ms clock period or 50ms high pulse width) to be visible to the human eye. A 640ns pulse is not visible. It is recommended to use a pulse stretching circuit on custom I/O board to detect high narrow pulse widths down to 500ns and stretch them to the visible width (e.g., >50ms).

The following Electronic Design web link article has a sample pulse stretching circuit:

http://electronicdesign.com/lighting/configurable-logic-chip-stretches-pulses-brighten-led-flash

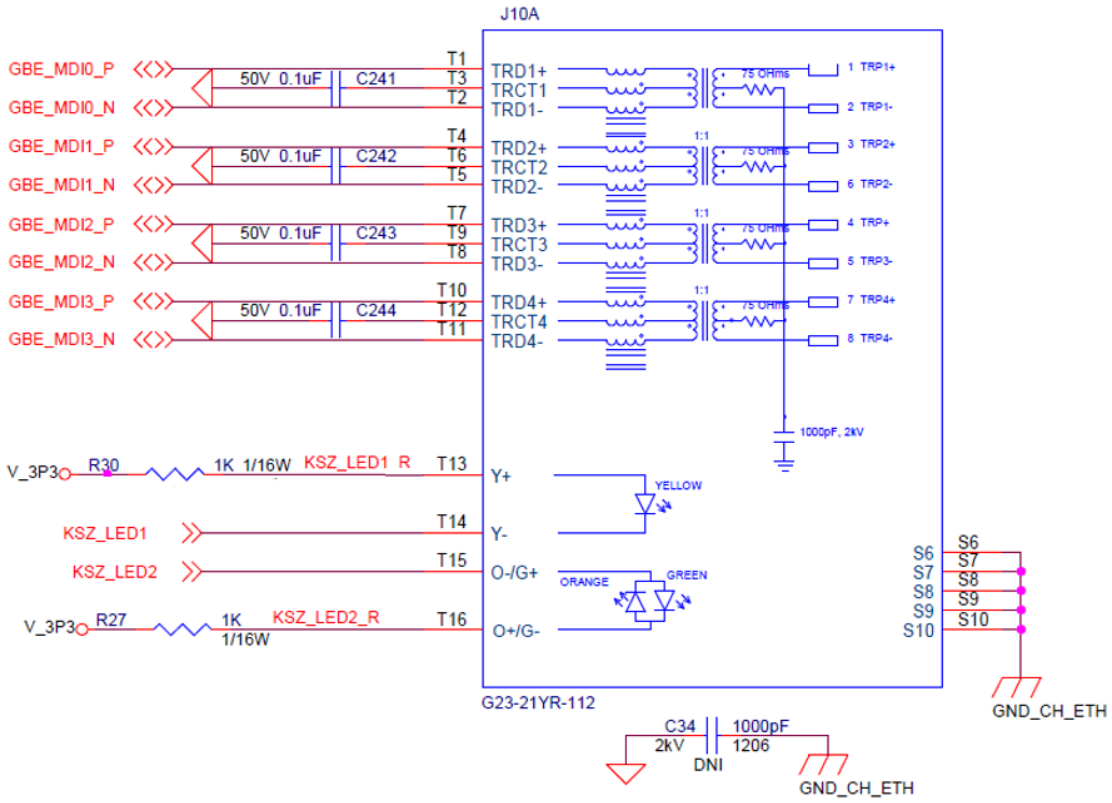

Figure 7: 1G LED Connections Sample Circuit

4.3.2 10G LED Configuration

Refer following sample circuit for LED signal connections.

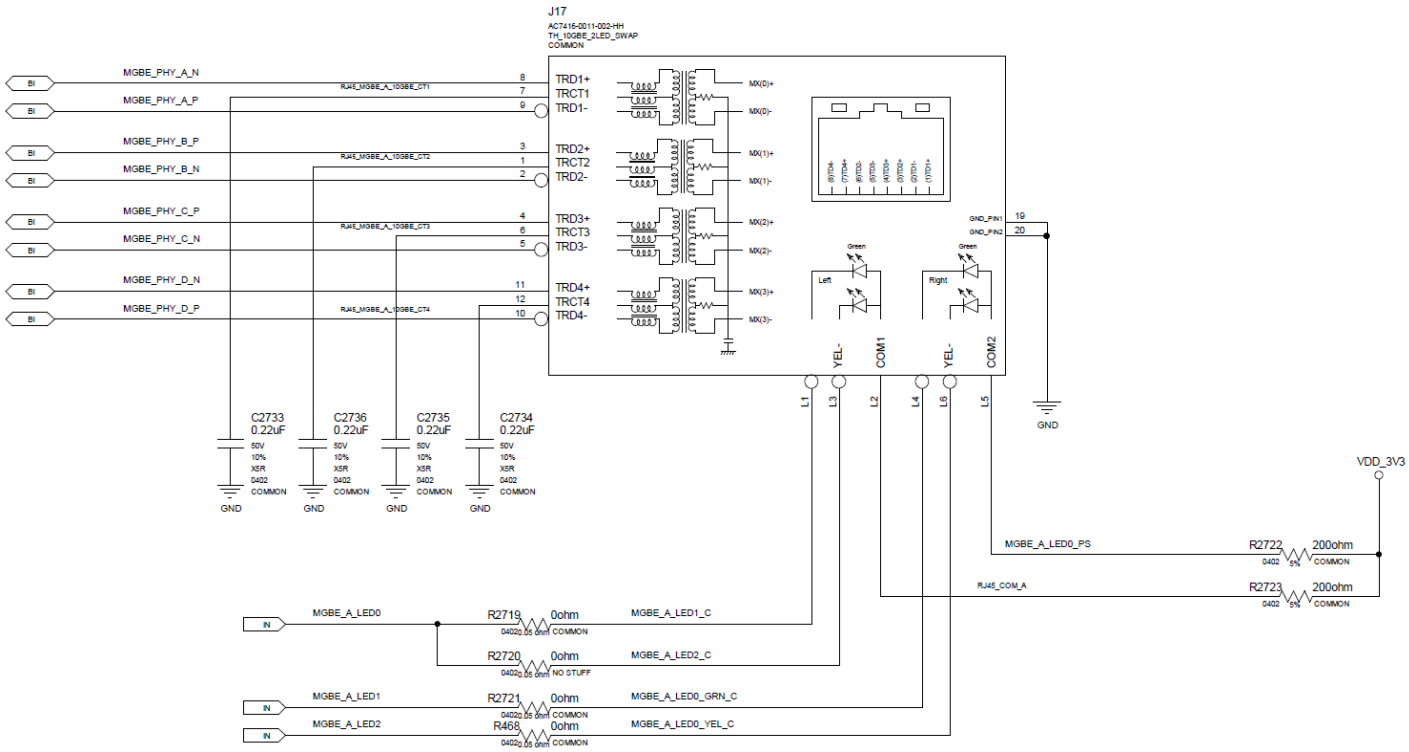

Figure 8: 10G LED Connection Sample Circuit

4.4 Display

The board offers one HDMI/DP video output option. The HDMI/DP port is directly from the Module and made available on the I/O connector.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
36	HDMI_DP2_TX0_CON_P	HDMI/DP Diff pair, AC coupled	DisplayPort 2 Lane 0 or HDMI Lane 2. AC-Coupled on Osbourne board.
38	HDMI_DP2_TX0_CON_N	HDMI/DP Diff pair, AC coupled	
42	HDMI_DP2_TX3_CON_P	HDMI/DP Diff pair, AC coupled	DisplayPort 2 Lane 1 or HDMI Lane 1. AC-Coupled on Osbourne board.
44	HDMI_DP2_TX3_CON_N	HDMI/DP Diff pair, AC coupled	
48	HDMI_DP2_TX2_CON_N	HDMI/DP Diff pair, AC coupled	DisplayPort 2 Lane 2 or HDMI Lane 0. AC-Coupled on Osbourne board.
50	HDMI_DP2_TX2_CON_P	HDMI/DP Diff pair, AC coupled	
54	HDMI_DP2_TX1_CON_N	HDMI/DP Diff pair, AC coupled	DisplayPort 2 Lane 3 or HDMI Clk Lane. AC-Coupled on Osbourne board.
56	HDMI_DP2_TX1_CON_P	HDMI/DP Diff pair, AC coupled	
39	GPIO20_DP/HDMI_EN_1P8	1.8 V	Can be used for HDMI/DP Power enable and termination selection through a load switch
41	DP2_AUX_CH_P	Open-Drain, 1.8V (3.3V tolerant)	Connect to HDMI DDC SCL or DP Aux+ through Level shifter
43	DP2_AUX_CH_N	Open Drain, 1.8V (3.3V tolerant	Connect to HDMI DDC SCL or DP Aux- through Level shifter
45	HDMI_CEC_CON	Open Drain, 1.8V (3.3V tolerant	Connect to HDMI CEC
47	DP2/HDMI_HPD	CMOS – 1.8V	Connect to HDMI port Hot Plug Detect pin. 10K pull-up to 1.8V is provided on Osbourne base board.

4.4.1 HDMI Configuration

By default, the configured display interface is HDMI. All the common choke, termination option and ESD protection circuitry are provided on the baseboard. In Figure 10 circuits marked in yellow box is implemented on Osbourne base board. The Custom I/O board should have required circuitry for I2C level shifting, load switch for enabling HDMI power along with the HDMI connector circuit.

Refer **Error! Reference source not found.** for more information on the protection circuit available on Osbourne board.

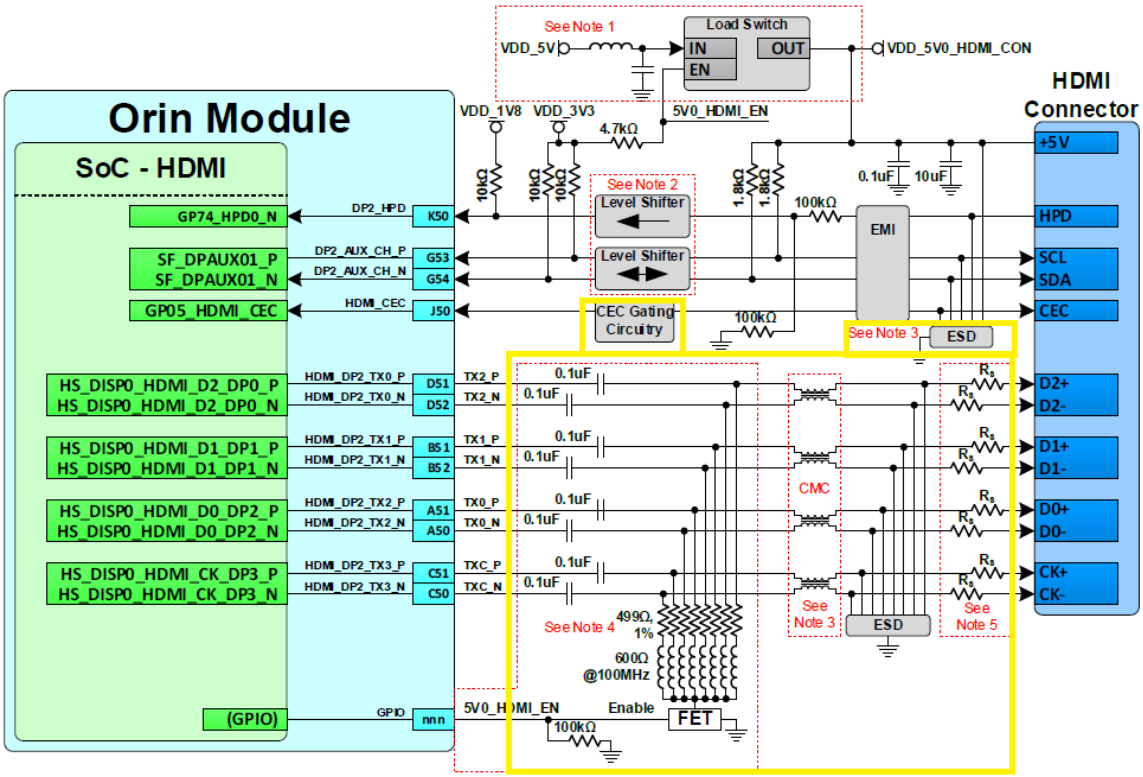

Figure 9: HDMI Configuration

Note 1: The load switch circuit shown is intended to remove power to the HDMI connector and related circuitry to avoid back drive on signals to the module. Other mechanisms may be used but must prevent module pins being driven when the module is off.

Note 2: Level shifters required on DDC/HPD. Orin module pads are not 5V tolerant and cannot directly meet HDMI VIL/VIH requirements. HPD level shifter can be non-inverting or inverting.

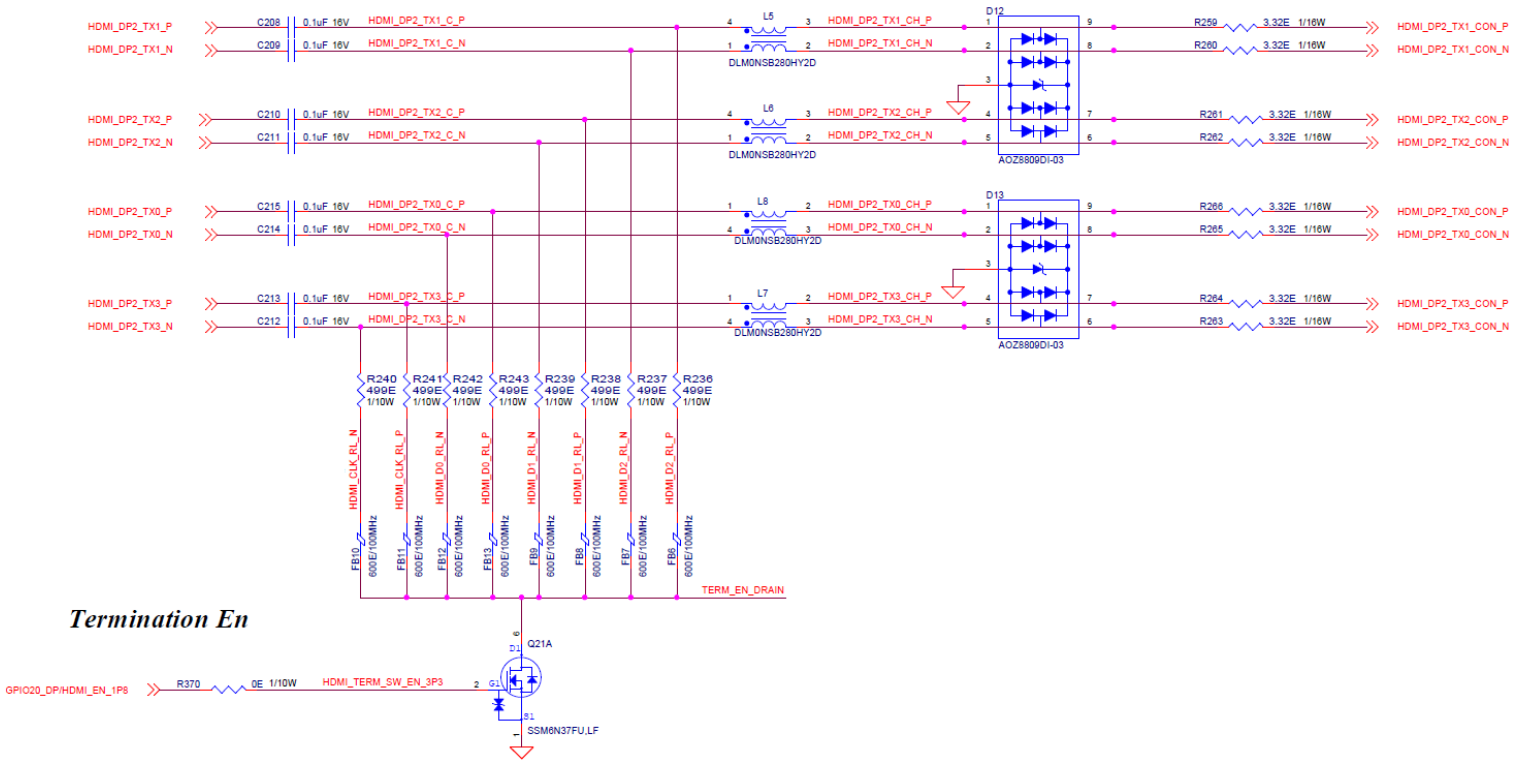

Figure 10: HDMI/DP Protection Circuit on Osbourne Board

Note: GPIO20_DP/HDMI_EN_1P8 should be driven low when used as Display Port (DP).

4.4.2 Display Port (DP) or eDP Configuration

The display interface can also be used in DP or eDP mode. Figure 11 shows display port connection example. The section marked in yellow box is implemented on the Osbourne base board. The load switch, level shifters, pull up/down configurations and connector need to be added on the custom IO board.

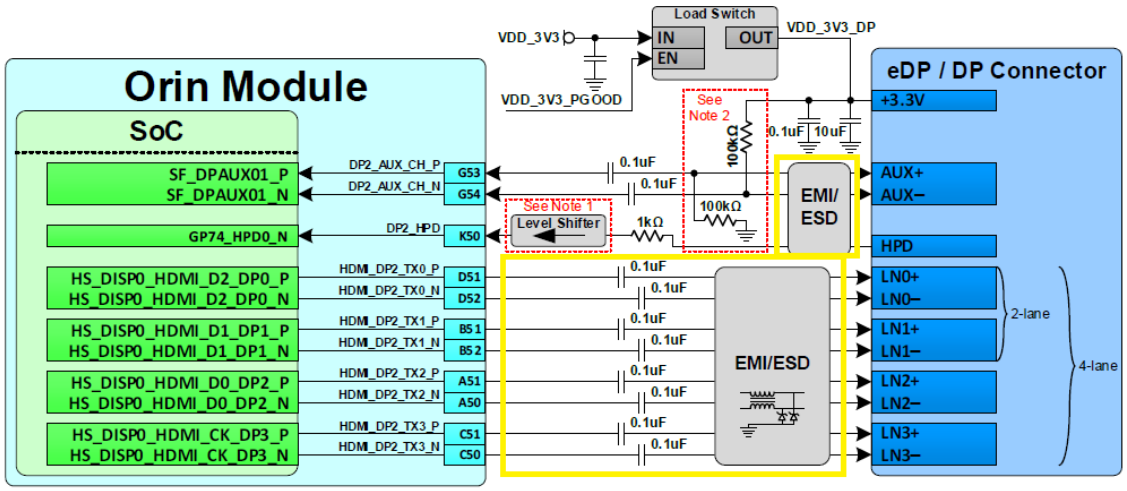

Figure 11: Display Port Configuration

Note 1: A Level shifter is required on HPD to avoid the pin from being driven when the module is off. The level shifter must be non-inverting (preserve polarity of the signal from the display).

Note 2: Pull-up/down only required for DP - not for eDP.

4.5 Audio

Audio I/O signals include stereo line out and mono/stereo mic in from the CODEC chip (Part# ALC5640). The audio signals made available on the I/O connector. The Custom I/O board should have suitable protection circuitry to protect against ESD or any other electrical transients. All audio signals should be routed referenced to GND_AUD on custom I/O board.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
1	AUDIO_HPOR_HDA	Analog Output	Headphone amplifier output right channel
3	AUDIO_HPOL_HDA	Analog Output	Headphone amplifier output left channel
2	GND_AUD	Audio Ground	Connect to low noise audio ground
4	AUDIO_MIC_L	1.8V, Analog Input	Connect to Analog Microphone left channel
6	AUDIO_MIC_R	1.8V, Analog Input	Connect to Analog Microphone right channel
8	AUDIO_PRSNT_L	1.8 V	Active low Input used to detect a valid audio device connection

4.6 Serial Ports

The board supports up to 4 serial ports from the module. Two serial ports, which can be configured as RS232 or RS422 or RS485 ports, are derived using single transceiver (Part#SP336EEY-L). The protocol selection is done through software control. Refer Osbourne user manual for more information about protocol selection. On board jumper option is provided to select termination (120 Ohm) for RS232/RS422/RS485 protocols. Refer section 265.1.1 for more information on jumper options.

Another Two fixed RS232 protocol ports are derived using another transceiver (Part#MAX3243EIPW). Fourth serial port does not support flow control feature.

Custom I/O board should have all required protection circuitry for the serial port signals.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
49	UART5_CTS_RS232	RS232 Signal	Serial Port 3: Connect to CTS pin on DB9 connector
51	UART5_RX_RS232	RS232 Signal	Serial Port 3: Connect to RX pin on DB9 connector
53	UART5_RTS_RS232	RS232 Signal	Serial Port 3: Connect to RTS pin on DB9 connector
55	UART5_TX_RS232	RS232 Signal	Serial Port 3: Connect to TX pin on DB9 connector
57	UART3_9_RX_RS232	RS232 Signal	Serial Port 4: Connect to RX pin on DB9 connector
59	UART3_9_TX_RS232	RS232 Signal	Serial Port 4: Connect to TX pin on DB9 connector
81	CTS2/RX2_N	RS232/ RS422	Serial Port 2: Connect to RS232 CTS2/RS422 RX2_N on DB9 connector
83	RX2/RX2_P	RS232/ RS422	Serial Port 2: Connect to RS232 RX2/RS422 RX2_NP on DB9 connector
85	RTS2/TX2_N/RX2_N	RS232/ RS422/ RS485	Serial Port 2: Connect to RS232 RTS2/RS422 TX2_P/ RS485 TX2+,RX2+ on DB9 connector
87	TX2/TX2_P/RX2_P	RS232/ RS422/ RS485	Serial Port 2: Connect to RS232 TX2/RS422 TX2_P/ RS485 TX2+,RX2+ on DB9 connector
89	CTS1/RX1_N	RS232/ RS422	Serial Port 1: Connect to RS232 CTS1/RS422 RX1_N on DB9 connector
91	RX1/RX1_P	RS232/ RS422	Serial Port 1: Connect to RS232 RX1/RS422 RX1_P on DB9 connector
93	RTS1/TX1_N/RX1_N	RS232/ RS422/ RS485	Serial Port 1: Connect to RS232 RTS1/RS422 TX1_N/ RS485 TX1-,RX1- on DB9 connector
95	TX1/TX1_P/RX1_P	RS232/ RS422/ RS485	Serial Port 1: Connect to RS232 TX1/RS422 TX1_P/ RS485 TX1+,RX1+ on DB9 connector

4.7 USB

The Osbourne board supports 1x USB2.0 via USB 2.0 hub routed to I/O connector. Three numbers of USB3.2 and three USB2.0 ports are also routed to the I/O connector. USB power switch, common choke and ESD protection circuitry are provided on the baseboard. One of the USB ports is shared with the PCIe when the Osbourne board work in configuration #2. Refer Nvidia AGB Orin design guide for more information on various configurations. Refer 5.1.3 for more information on jumper configurations. Figure 12 and Figure 13 shows the USB protection circuit available on the Osbourne board for USB2.0 and USB3.2 interfaces respectively.

I/O Conn. Pin	Orin Module Connector Pin No.	Signal Name	Voltage Level/Pin Type	Description
27	NA	V_USB3_1	Power: 5.0V	Connect to V+ pin on USB3.2 Port 0 connector
29	C10	USB2_D1_CH_N	USB2 Diff pair	Connect to D+ pin on USB2.0 Port 2 connector
31	C11	USB2_D1_CH_P	USB2 Diff pair	Connect to D- pin on USB2.0 Port 2 connector
33s	NA	V_USB3_2	Power: 5.0V	Connect to V+ pin on USB3.2 Port 1 connector
35	F13	USB2_D0_CH_N	USB2 Diff pair	Connect to D+ pin on USB2.0 Port 1 connector
37	F12	USB2_D0_CH_P	USB2 Diff pair	Connect to D- pin on USB2.0 Port 1 connector
61	NA	V_USB2_VBUS	Power: 5.0V	Connect to D+ pin on USB2.0 Port 4 connector
63	G10*	USB2_HUB_D4_CH_N	USB2 Diff pair	Connect to D- pin on USB2.0 Port 4 connector
65	G11*	USB2_HUB_D4_CH_P	USB2 Diff pair	Connect to D- pin on USB2.0 connector
67	NA	V_USB3_3	Power: 5.0V	Connect to V+ pin on USB3.2 Port 2 connector
69	A11	USB2/PCIE_CLK_CH_N	USB2 Diff pair/ PCIe Diff pair	Connect to D+ pin on USB2.0 Port 3 connector
71	A10	USB2/PCIE_CLK_CH_P	USB2 Diff pair/ PCIe Diff pair	Connect to D- pin on USB2.0 Port 3 connector
12	A22	USB3/PCIE_UPHY_RX0_P	USB3 / PCIe Diff pair	Connect to RX+ pin on USB3.2 Port 1 connector
14	A23	USB3/PCIE_UPHY_RX0_N	USB3 / PCIe Diff pair	Connect to RX- pin on USB3.2 Port 0 connector
18	J22	USB3/PCIE_UPHY_TX0_P	USB3 / PCIe Diff pair	Connect to TX+ pin on USB3.2 Port 0 connector
20	J23	USB3/PCIE_UPHY_TX0_N	USB3 / PCIe Diff pair	Connect to TX+ pin on USB3.2 Port 0 connector
24	C23	USB3_UPHY_RX1_P	USB3 Diff pair	Connect to RX+ pin on USB3.2 Port 1 connector
26	C22	USB3_UPHY_RX1_N	USB3 Diff pair	Connect to RX- pin on USB3.2 Port 1 connector
30	G23	USB3_UPHY_TX1_P	USB3 Diff pair	Connect to TX+ pin on USB3.2 Port 1 connector
32	G22	USB3_UPHY_TX1_N	USB3 Diff pair	Connect to TX+ pin on USB3.2 Port 1 connector
60	C34	USB3_UPHY_RX20_P	USB3 Diff pair	Connect to RX+ pin on USB3.2 Port 2 connector
62	C35	USB3_UPHY_RX20_N	USB3 Diff pair	Connect to RX- pin on USB3.2 Port 2 connector
66	K32	USB3_UPHY_TX20_P	USB3 Diff pair	Connect to TX+ pin on USB3.2 Port 2 connector
68	K33	USB3_UPHY_TX20_N	USB3 Diff pair	Connect to TX+ pin on USB3.2 Port 2 connector

*Not direct connection from Orin module, connected through USB hub circuit

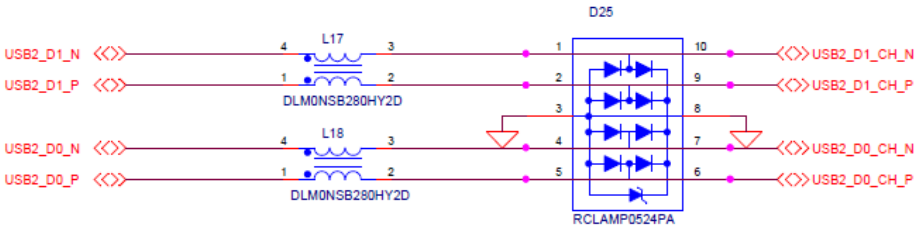

Figure 12: USB2.0 Circuit on Osbourne Board

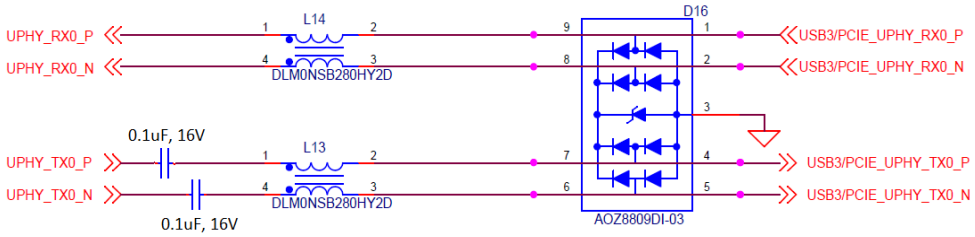

Figure 13: USB 3.2 Circuit on Osbourne Board

Note: USB3.2 Port 0 is shared between USB and PCIe. In configuration#1 it is used as USB3.2 and in configuration#2 it is used as PCIex1(C0) port. Refer 5.1.3 for more details on jumper configurations on Osbourne base board.

4.8 Digital I/O

The board provides 8 digital I/O's, which are individually configurable as an output or input. The I/Os are routed to the I/O connector. Figure 14 shows the ESD protection provided on the GPIO lines. Additional protection circuits shall be implemented on Custom I/O board as needed.

Provision is to select the DIO Voltage level of 3.3/5V and configure Pull up (10K) and pull down(10K) though the Jumper JP2 is provided. Refer 5.1.2 for more information on jumper configuration.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
11	DIO_PA7	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
13	DIO_PA6	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
15	DIO_PA5	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
17	DIO_PA4	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
19	DIO_PA3	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
21	DIO_PA2	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
23	DIO_PA1	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin
25	DIO_PA0	V_DIO (3.3V or 5V)	Bi-directional general purpose I/O pin

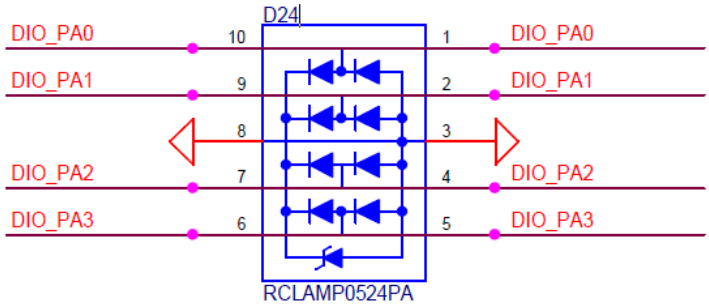

Figure 14: ESD protection on Digital IO Signals

4.9 CAN

The board provides two CAN interface from the AGX Orin module to the I/O connector. The CAN transceiver used (Part# MCP2551T-I/SN) supports baud rates from 60 kbaud up to 1 Mbaud. Bi-directional TVS diodes and noise filter circuits are provided on the Osbourne board. Refer Figure 15 for more information on protection available on the CAN bus signals.

I/O Conn. Pin	Signal Name	Voltage Level/Pin Type	Description
73	CAN1_L	CAN Differential Pair	Connect to CAN LOW line on the CAN BUS
75	CAN1_H	CAN Differential Pair	Connect to CAN HIGH line on the CAN BUS
77	CAN0_L	CAN Differential Pair	Connect to CAN LOW line on the CAN BUS
79	CAN0_H	CAN Differential Pair	Connect to CAN HIGH line on the CAN BUS

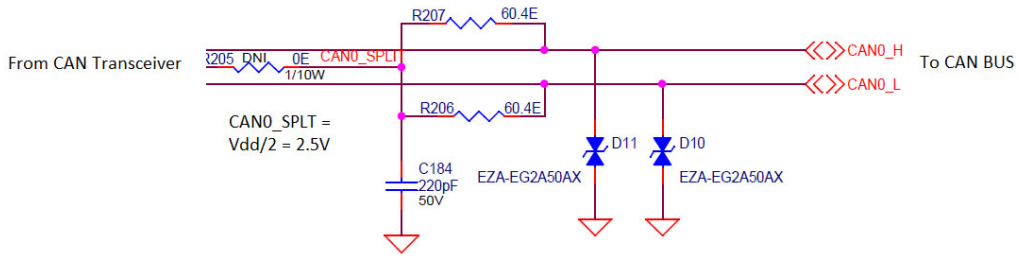

Figure 15: CAN filter and protection circuits on Osbourne Board

4.10 SPI

SPI signals are connected to the I/O connector for interfacing external device. On board 1.8V to 3.3V level translator (Part#TXB0108DQSR / NLSX3018MUTAG) shifts SPI signals to 3.3V level. Custom I/O board should have ESD diodes, or any other protection circuitry as needed. Refer Nvidia AGX Orin product design guide for more information on specifications.

I/O Conn. Pin	Orin Module Connector Pin No.	Signal Name	Voltage Level/Pin Type	Description
121	J57	SPI1_SCK_3P3	3.3 V	SPI 1 Serial clock – connect to slave clock pin
123	E55	SPI1_CS0_3P3	3.3 V	SPI 1 chip select – connect to slave select pin
125	A56	SPI1_MISO_3P3	3.3 V	SPI 1 master in slave out – connect to slave MISO line
127	D55	SPI1_MOSI_3P3	3.3 V	SPI 1 master out slave in – connect to slave MOSI line

4.11 I2C

I2C signals are connected to the I/O connector for interfacing external device. On board 1.8V to 3.3V level shifter circuit (Part#TXB0108DQSR / NLSX3018MUTAG) shifts I2C signals to 3.3V level. 2K pull-ups to 3.3V are also provided on both I2C clock and Data lines on Osbourne base board. Custom I/O board should have ESD diodes, or any other protection circuitry as needed. Refer Nvidia AGX Orin product design guide for more information on specifications.

I/O Conn. Pin	Orin Module Connector Pin No.	Signal Name	Voltage Level/Pin Type	Description
97	E60	I2C_GP8_DAT_3P3	I2C data; 3.3 V	Connect to I2C bus serial data
99	D61	I2C_GP8_CLK_3P3	I2C Clock; 3.3 V	Connect to I2C bus serial clock

4.12 Power and System Signals

Power and system signal pins such as Power button, Force recovery, Reset are available on the IO connector. Refer Nvidia AGX Orin product design guide for more details. Memory erase signal for M.2 Key M SSD is also available on I/O connector.

I/O Conn. Pin	Orin Module Connector Pin No.	Signal Name	Voltage Level/Pin Type	Description
101	L61*	BUTTON_POWER_ON_N	3.3 V	Low Input from push button switch enables the power to the system. This feature is currently not enabled on Osbourne base board. Refer Nvidia AGX Orin module design guide for more details.
103	L60	SYS_RST_IN_N	Open Drain, 1.8V	When asserted, the SoC, eMMC, & QSPI are in reset. Refer Nvidia AGX Orin module design guide for more details.
105	L10	FORCE_RECOVERY#	CMOS – 1.8V	Force Recovery strap pin: Held low when SYS_RESET_N goes inactive (power-on or reset button press) to enter force recovery mode. Force recovery mode is used to program Orin module through USB2.0 USB0N/P or USB3.2 port#1. Refer Nvidia AGX Orin module design guide for more details.
111	B9	PEX_C1_RST_N	Open-Drain, 3.3V	PCIe Reset for controller #0. 4.7KΩ pull-up to 3.3V on Orin module. This pin is used to reset end point device when UPHY_RX0/TX0 is configured as PCIe x1 (C0) port instead of USB3.2 port.
113	NA	MEM_ERS_GPIO	1.8 V	Connected to Pin 6 and 8 of M.2 M Key connector. This functionality is module specific and can be used only on supported modules.

*Not direct connection to Orin module, connected through power sequencer circuit

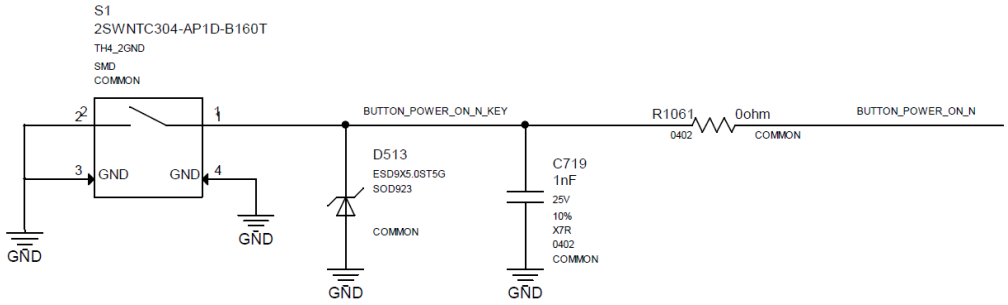

Figure 16: Button Power ON Sample Circuit

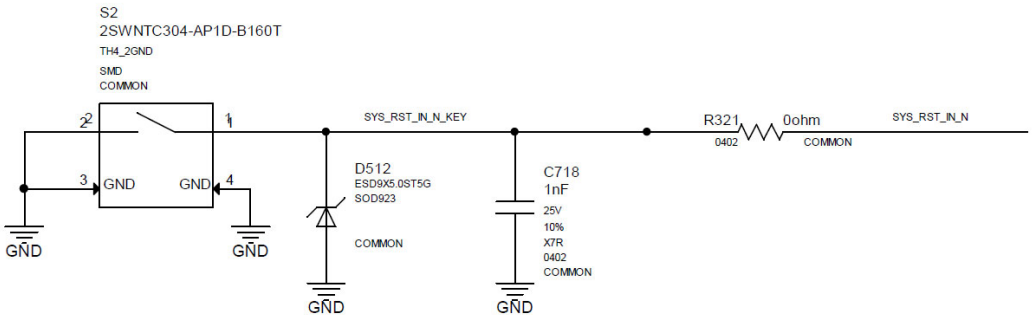

Figure 17: Reset Circuit Sample

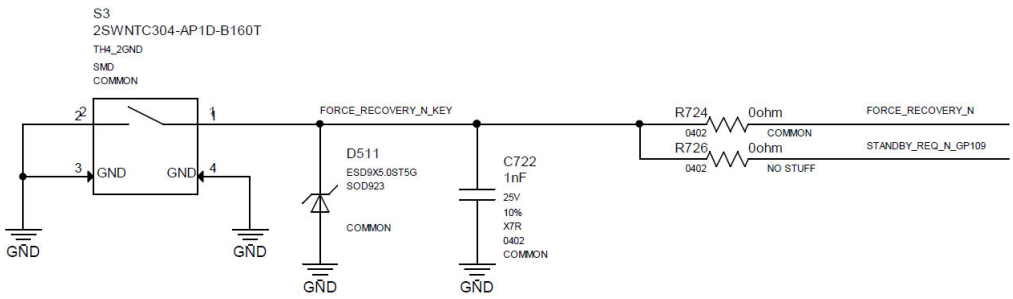

Figure 18: Force Recovery Sample Circuit

Note: 1nF debouncing capacitor is already available on the Osbourne base board on SYS_RST_IN_N, FORCE_RECOVERY# and BUTTON_POWER_ON_N signals.

4.13 Additional Control GPIOs

Osbourne board provides following GPIOs which can be used for general purposes.

I/O Conn. Pin	Orin Module Connector Pin No.	Signal Name	Voltage Level/Pin Type	Description
115	A48	SER_GPIO_SEL	1.8 V	General purpose IO pin from Orin Module. Used as input for multiplexing digital IO and Serial port 2 signals on IO board using analog switch/mux.
117	H52	CAN_SER_SEL2	1.8 V	General purpose IO pin from Orin Module. Used for multiplexing CAN0 and UART5 signals on IO board using analog switch/mux.
119	D54	CAN_SER_SEL1	1.8 V	General purpose IO pin from Orin Module. Used for multiplexing CAN1 and UART3 signals on IO board using analog switch/mux

5. APPENDIX

5.1 Jumper Configuration on Osbourne Base Board

5.1.1 JP1 Jumper Configuration

JP1 Jumpers Configuration are provided enable and disable the termination of serial ports1-2.

Position	Function	IN	OUT
TX1	121E Termination Enabled for SER1 TX RS-485/RS-422 Mode	Enabled	**Disabled***
RX1	121E Termination Enabled for SER1 RX RS-485/RS-422 Mode	Enabled	**Disabled***
TX2	121E Termination Enabled for SER2 TX RS-485/RS-422 Mode	Enabled	**Disabled***
RX2	121E Termination Enabled for SER2 RX RS-485/RS-422 Mode	Enabled	**Disabled***
***Default Mode**			

5.1.2 JP2 Jumper Configuration

JP2 Jumpers are provided to select the voltage level and Pullup/pull down configuration of the DIO. By default, the DIOs are 3.3 Volare pulled down. The configuration is as shown below:

Position	Function	IN	OUT
5V	DIO Voltage Level	5V	
3V3	DIO Voltage Level	**3.3V***	
PU	DIO Pull up Enable	Enabled	Disabled
PD	DIO Pull down Enable	**Enabled***	Disabled
***Default Mode**			

Note: Make sure 5V and 3V3 Jumper are not IN at same time.

5.1.3 JP3 Jumper Configuration

JP3 Jumpers Configuration are provided to select the Boot configuration, x16 PCIe or MINICARD, Wake on LAN selection and auto power selection. The configuration is as shown below:

Position	Function	IN	OUT
PCIE	x16 PCIE / MINICARD Selection	x16 PCIE	**MINICARD***
CFG	Boot Configuration	Config #2	**Config #1 ***
WOL	Wake on LAN	Enabled	**Disabled***
AUTO	Auto Power	Enabled	**Disabled***
***Default Mode**			